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load + miss + (stall or stop or cease or halt) ·

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... example, to implement complete opcodes such as floating point arithmetic instructions or hardware multiply and divide. This particular ...

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... the Grand, and it was a regular **stop** on the ... there were colourful fruit and vegetable **stalls**, in front of which the ... If the engine sputtered to a **halt** and the driver ...

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... where the day- time hawkers set up their **stalls**, vegetable husks ... there was no canopy over the rear **load** area. ... had retreated and were now hoping to **stop** a river ...

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... After landing, the plane rolled out over a washboard of a runway, clanking to a **stop** straight ahead where we waited for a fuel truck. ...

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... Hit/miss/way miss ... the bypassed result becomes available from the functional unit

or load. ... A single cluster has the two floating-point execution pipes, with a ...

Cited by 405 - [Related Articles](#) - [Web Search](#) - [BL Direct](#)[The Alpha 21264 microprocessor architecture - group of 2 »](#)RE Kessler, EJ McLellan, DA Webb - Computer Design: VLSI in Computers and Processors, 1998. ..., 1998 - [ieeexplore.ieee.org](#)

... the minimum three for an integer load hit that ... on cycles when there is a load miss,

otherwise it ... The 21264 treats floating-point loads differently than integer ...

Cited by 177 - [Related Articles](#) - [Web Search](#)[Superscalar instruction execution in the 21164 Alpha microprocessor - group of 4 »](#)JH Edmondson, P Rubinfeld, R Preston, V ... - Micro, IEEE, 1995 - [ieeexplore.ieee.org](#)

... A floating-point divider connects to the add pipeline, and, except for the issue

cycle and a ... This unit buffers load instructions that miss in the ...

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... For floating-point load instructions, the data is written to the register file using ...

missed, the conflict is resolved by forcing the new load to miss in the ...

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... 7000 came from: Miss Address File merging (load miss merging) of ... I/D caches show

a high miss rate. ... Alpha 21164 doubles the number of floating-point and integer ...

Cited by 48 - [Related Articles](#) - [Web Search](#)[Itanium 2 processor microarchitecture - group of 26 »](#)C McNairy, D Soltis - Micro, IEEE, 2003 - [ieeexplore.ieee.org](#)

... The ALAT enables a load to advance beyond ... logic Exception detect L2D TLB miss; L2

cache resources unavailable for memory operations; floating-point and integer ...

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... buffering in the I stage (the miss queue). ... cycle of floating-point instructions M

Load data alignment ... Moving the floating-point unit away from the integer core ...

Cited by 71 - [Related Articles](#) - [Web Search](#) - [BL Direct](#)[The PowerPC 620 microprocessor: a high performance superscalar RISC microprocessor - group of 2 »](#)D Levitan, T Thomas, P Tu - Comcon'95. Technologies for the Information Superhighway, ..., 1995 - [ieeexplore.ieee.org](#)

... Load, store, branch, and floating-point instructions flow through the pipeline somewhat

differently than integer instructions as illustrated in the figure. ...

Cited by 39 - [Related Articles](#) - [Web Search](#) - [BL Direct](#)[A high speed superscalar PA-RISC processor - group of 3 »](#)E DeLano, W Walker, J Yetter, M Forsyth - Comcon Spring 92. Thirty-Seventh IEEE Computer Society ..., 1992 - [ieeexplore.ieee.org](#)

... The "Hit under Miss" feature applies to both integer and floating point LOADs and ...

execution halts when the target register of a LOAD miss is needed as ...

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D Leibholz, R Razdan - Proc. IEEE Comcon - doi.ieeeecs.org

... data can be supplied to load instructions (bypassed ... I Memory references which miss

the internal caches and ... and issues them to the two floating point pipelines. ...

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